EEL 5322 VLSI CIRCUITS AND TECHNOLOGY SYLLABUS

Course Outline: (See Course Video Lectures Tab for Streaming Videos and Video Downloads)

Weekly Date, (No. of Classes) Class topics, Readings, In Class Notes in pdf form.

08/25 (3) Syllabus, What is VLSI; Class 1 Notes, Statistics Review, CMOS X-section, Survey and Permission Form, Class 2 Notes CMOS Technology, Gaussian Analysis Handout Statistics Web References, Implant Concept Graphics, Ion Implant Web references, Class Notes 3 Ion Implantation, Ion Implant Range Tables

LTSPICE Information

LTSPICE Model Instilation

LTSPICE MOS modeling file

Read Chap. 2 .1, 2.2 and 2.3 of Rabaey, 1.2, 1.3.1

In Class Notes Lecture 1, In Class Notes, Lecture 2, In Class Notes Lecture 3


Read Chap. 5 .1, 5.2, 5.3, 5.4 of Jaeger and Chap. 4.1, 4.2, 4.3, 4.4, 4.5, 4.6 of Jaeger

In Class Notes Lecture 4, In Class Notes Lecture 5,

09/08 (3) Lecture 6 Notes Diffusion, Lecture 6 Diffusion Calculations, Oxidation Web References, Class 7 Notes Oxidation, Class 8 Notes Oxidation, Class 8 Oxidation Example, Deposition Web References

Read Chap. 3.1, 3.2, 3.3, of Jaeger and Read Chap. 6.1, 6.2, 6.3

In Class Notes Lecture 6, In Class Notes Lecture 7, In Class Notes Lecture 8,

09/15 (3) Class 9 Notes, Class 9 Graphics, Class 9 Example, CMP_Web_References, Class_10_Notes, Class_10_Article, Class_10_Graphics, Etch Web Reference, Class 11 Notes, Etch Calculation, Photolithography Web References

Read Chap. 6.1, 6.2, 6.3 and Chap. 7.7, 7.8, 3.8.2 of Jaeger

In Class Notes Lecture 9, In Class Notes Lecture 10, In Class Lecture 11
09/22 (3) Class Notes 12, Photolithography System Graphics, Photolithography Web References, Class Notes 13, A Little Light Magic Reference, Alignment Web Reference, Photomasks, Class Notes 14, CD Yield Example Calculation, Yield Web References, Yield Calculation

- Read Chap. 2.1, 2.2, 2.3, 2.4, 2.5 of Jaeger, Chap. 1.3.1, 1.3.2, 9.1, 9.3.5 of Rabaey
- In Class Lecture 12, In Class Lecture 13, In Class Lecture 14

09/29 (3) Class Notes 15, CD Yield Calculations, Alignment Tree Web Reference, Class Notes 16 CMOS Flow, Rabaey CMOS Flow, Class Notes 17 Isolation and Latch-up,

- Read Chap. 8.7 of Jaeger and Chapter 2.2 Rabaey
- In Class Lecture 15, In Class Lecture 16, In Class Lecture 17

10/6 (3) CMOS Design Rules 1, Design Rules 1 with color, Exam 1

- Read Chapter 1 Rabaey
- In Class Lecture 18, In Class Lecture 19

10/13 (3) Cadence Links, Cadence Design Startup, Design Rules 2, MOSIS 250nm CMOS Link, Homework 13 ungraded,

- Exam 1 Solution
- Cadence Tutorial Slides
- Read Chap. 4.1 to 4.3 and Chap. 3.3 of Rabaey and 9.2, 9.3 Jaeger
- In Class Lecture 20, In Class Lecture 21,

10/20 (3) Technology Cross-sections Class Notes, MOSIS t375b lo Parameters, Homework 14, Resistance, Homework 15, Rabaey Corrections, Lecture MOS Transistors, MOS Transistors II

- Read Chap. 3.3 and Chap. 5 of Rabaey
- In Class Lecture 22, In Class Lecture 23, In Class Lecture 24,

10/27 (3) Capacitance, Inverter Static Characteristics, Inverter Dynamic Characteristics, Inverter Delay, Homework 16 Inverter Design,

- Read Chap. 5 of Rabaey
- In Class Lecture 25, In Class Lecture 26, In Class Lecture 27,
11/3 (3) CMOS Compound Gates, Compound Gates I, Compound Gates II, SRAM Project due Dec. 10, SRAM Noise Margin Simulation

Read Chap. 6 of Rabaey

In Class Lecture 28, In Class Lecture 29, In Class Lecture 30,

11/10 (3) Pass Transistor Logic, Dynamic Logic, Exam II

Read Chap. 6 of Rabaey:

In Class Lecture 31, In Class Lecture 32,

11/17 (3) Domino Logic, Domino Logic I, Memory I, Memory II, Memory III, Memory IV

Read Chap. 12 of Rabaey

In Class Lecture 33, In Class Lecture 34, In Class Lecture 35,

11/24 (1) Pseudo NMOS, Ratioed Logic Slides, (Thanksgiving Holiday Nov. 26 through Nov. 28, 2014)

Exam II Solution,

Read Chap. 12 of Rabaey

In Class Lecture 36,

12/1 (3) CMOS Logic Slides, Technology Scaling Slides, Exam III

Read Chap. 6 of Rabaey

In Class Lecture 37, In Class Lecture 38

12/8 (2) CMOS Testing, CMOS Testing II CMOS Testing III, (Study days Dec. 5 and Dec. 6, 2013) Projects due Wednesday Dec 10.

In Class Lecture 39, In Class Lecture 40

There is no final exam.

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Class Period and Location: 6th period, MWF, 12:50 to 1:40pm, Room NEB 100.

Office Hours: MWF 1:45 pm to 2:45 pm

TA: Dooyoung Kim and TBA


Course Goals: To develop proficiency in analyses, design and implementation of CMOS circuits. To develop understanding of interdependence of CMOS circuit design with process technology and IC manufacturing. To be a designer in modern CMOS processes with high level of manufacturing variations.

EDGE Students: The EDGE studio will post recorded lectures in the Course Video Lectures section of Sakai (see tabs on the left of the screen). I will give you up to 3 extra days (72 hours) to complete and turn in class assignments and Quizzes during the regular semester. There will be three in class exams and no final exam.

Course Materials: I will be using the Syllabus to index of the daily class materials posted for you to review and to learn from. So, you can find most learning materials by clicking on a link from the Syllabus. I try to post all written materials and video materials used in the lectures to assist in your learning. I also post class lecture materials at least 24 hours ahead of time. I post 5 years of old quizzes or exams a week before the in class quiz. There will be folders that contain course materials (Course Notes, Old Exams, Cadence notes, In Class Notes, etc) in the Resources section of Sakai (see tabs on the left of this section).
**Computer and Software Required:**
Workstations with CADENCE Design system on campus, off-campus can use X-Windows or an X-terminal on a high-speed internet link to UF Campus Computers, or can use equivalent IC design software.

All students are required to have a Gator link account and use Sakai for course handouts, grade information, course notices, etc., see e-learning support services

**Course Study Requirements:**
Students are responsible to study all in class materials including those written on the board and presented orally, all Class Handouts all assigned readings, all projects and homework. Absence from class can result in missing materials tested on exams.

**Attendance and Expectations:** Attendance is not required except for on-campus students during the exams. This is an EDGE course so students are required to watch the class video for each lecture. There is a no wireless device policy (no cell phones, smart phones, computers, tablets, etc.) during exams.

**Catalog Description:** Introduction to VLSI circuit technology and manufacturing. Fabrication, device models, layout, parasitics, and simple gate circuits.

**Make Up Exam Policy:** Students are expected to attend exams at the scheduled times. Exams can be made up if there is a genuine medical emergency with a doctor's or clinic medical note or a family emergency with some documentation. Students are NOT excused from exams for job interviews and early holiday travel home. Students with other non-emergency exam scheduling issues must obtain permission from the instructor prior to missing an exam.

**Work Requirements:**

- Homework
- Computer Laboratories and projects
- Exams: Quizzes, Midterms and Final

**Examinations:** Quizzes as assigned
- Midterm 1: Tentatively, First week of October
- Midterm 2: Tentatively, Last week of October/First week of November.
- Midterm 3: Tentatively, First week of December

Grades will be on a curve and your relative statistical performance to the class average grades counts, not your absolute numerical performance. For example, if you have a 91 average and the class median is 90 (not likely) you will get a B. You must be significantly better than average to get an A.

**Passing Grades and Grade Points Effective Summer A 2009**
Letter Grade
A  A-  B+  B  B-  C+  C  C-  D+  D  D-  E  F  I  N  G  S-
Grade U
Points 4.0 3.67 3.33 3.0 2.67 2.33 2.0 1.67 1.33 1.0 67 0 0 0 0

Preliminary Grading Policy:
Homework and Projects - 15%
Midterms and Quizzes - 85%

Academic Honesty:
All students admitted to the University of Florida have signed a statement of academic honesty committing themselves to be honest in all academic work and understanding that failure to comply with this commitment will result in disciplinary action.

This statement is a reminder to uphold your obligation as a student at the University of Florida and to be honest in all work submitted and exams taken in this class and all others.

Students requesting classroom accommodation must first register with the Dean of Students Office. The Dean of Students Office will provide documentation to the student who must then provide documentation to the instructor when requesting accommodation.